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Accordingly, independent claim 1 has been amended to cancel the element, "a plurality of scan lines...," and to add the element, "a plurality of probe lines...," from claim 2. In rejecting claim 2, the Examiner stated, "Rajski and Mori do not teach a plurality of probe lines for carrying system operation signal at predetermined probe points. Gheewala teaches a programmable interface apparatus for coupling test signal from internal test matrix including a plurality of probe lines for setting logic states at internal circuit elements.... It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Mori with the teachings of Gheewala to include a programmable interface as taught by Gheewala into the built in self test circuitry as taught by Mori to provide a built self test circuitry having a programmable interface with a plurality of probe lines for carrying system operation signal at predetermined probe points because it would provide the advantages that the test signals are loaded into internal probe points without the need for complex scan registers...."

The applicants do not see how the combination of the cited Rajski, Mori and Gheewala patents teaches the claimed invention as recited in amended claim 1 and respectfully disagree with the Examiner's conclusion. In the first place, the Examiner appears to be confused by similar terminology in the Gheewala patent and the applicants' claim. Applicants' probe lines "...carry[ing] system operation signals at predetermined probe points of said logic blocks...." On the other hand, Gheewala's probe lines are used for carrying control signals, not system operation signals. In the test matrix 18, "a probe line 32 is coupled to a switch 36 for defining the switch "ON" or "OFF" state." Col. 4, lines 25-26. In the description of the interface circuit 12, "Signals P1, P2 are probe lines signals from the test matrix 18....When probe line signal P1 is active..., sense line signal S1 is passed through transistor 58. When probe line signal P2 is active..., sense line signal S2 is passed through transistor 60." Col. 5, lines 56-62.

Secondly, even assuming that the Examiner analogizes the sense lines carrying signals S1 and S2 to the applicants' probe lines, the combination of the cited Rajski, Mori and Gheewala patents still do not teach the applicants' claimed invention. The probe lines of claim 1 carry "system operation signals at predetermined probe points of said logic blocks, said system operation signals stored in said memory so that said system operation signals are

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retrievable." On the other hand, the interface circuits 12 of the cited Gheewala patent may carry input system operation signals directly into operational circuitry 16 from primary input pins 14a-14c, or carry output system operation signals directly out of operational circuitry 16 to the primary output pins 14d-14f, in normal operation of the integrated circuit 10. See col. 3, lines 56-63, for example. No memory is involved. Alternatively, the interface circuits 12 may carry a <u>test</u> signal response from the data register 22 to the primary output pin, or to a second operational circuit. See col. 5, lines 36-39 and lines 44-47. The data register 22, which the Examiner would presumably analogize to applicants' "memory" element, stores test signal responses, not system operation signals as recited in claim 1.

Finally, as the applicants understand the cited Gheewala patent, Gheewala *et al.* teaches programmable interface circuits for normal input/output (I/O) operation, and also for test mode operation to observe or set probe points in the operational circuits 16 of an integrated circuit 10. Gheewala does not teach the execution of normal operation of the integrated circuit while simultaneously observing the probe points in operation. The applicants do. What is observed are the system operation signals, the signals of normal system operations, not test signals (or test signal responses). Claim 1 recites, "…a plurality of probe lines responsive to said control unit carrying system operation signals at predetermined probe points of said logic blocks, said system operation signals stored in said memory…so that said system operation signals are retrievable." To further make their point, the applicants have added new dependent claims 20 and 21 recite that the recited system operation signals comprise "sequential system operation signals," and "sets of sequential system operation signals," respectively. It should be evident that the probe lines (actually sense lines) of the Gheewala patent do not carry system operation signals as claimed by the applicants.

Hence, as amended, claim 1 should be allowed. Neither the cited Rajski, Mori and Gheewala patents singly, nor in combination, teach the recited invention. Claims 2-9, which are dependent upon independent claim 1, are allowable for at least being dependent upon an allowable base claim, as argued above. The claims are also allowable in their own right.

For example, amended dependent claim 6, now dependent upon claim 1 recites that "each of said probe lines comprises a string of programmable connectors providing a

signal path for carrying system operation signals at predetermined probe points of said logic

blocks in one mode." In rejecting claim 6, the Examiner stated, "Gheewala teaches each of

said probe lines comprises a string of programmable connectors [Fig. 3] providing a signal

path for carrying system operation signals at predetermined probe points of said logic blocks in

one mode [col. 2 lines 42-63]." As explained above, the probe lines of Gheewala carry control

signals; rather the sense lines of Gheewala carry data. See col. 2, lines 47-48. The applicants

understand that the latch being referred to is latch 68 in Fig. 3. However, if the sense/control

lines 34 of the test matrix 18 of Fig. 2, which carry the signals S1 and S2, are considered to be

the applicant's probe lines, the applicants are confused as to the location of "the string of

programmable connectors" which comprise each probe line. The cited Gheewala patent does

not teach the applicant's invention, as recited in claim 6. Likewise, it should be apparent that

claims 7-9 are not taught by Gheewala either.

Previously pending claims 10-14 were rejected under 35 USC §103(a), as being

obvious over the combination of the previously cited Mori patent in view of the previously

cited Gheewala patent. Independent claim 10 has been amended to address the Examiner's

concerns under 35 USC §112, second paragraph. Furthermore, the applicant also corrected

language in the claim to now read, "a unit...for capturing sets of sequential system operation

signals...." In rejecting claim 10, the Examiner found that, "Mori does not teach a plurality of

probe lines coupled to predetermined probe points of said integrated circuit," and then cited the

Gheewala patent in the same manner as for previously pending claim 2. As argued above with

respect to amended independent claim 1, the Gheewala patent does not teach the "plurality of

probe lines...", as recited in claim 10.

The applicants also traverse the Examiner's analysis of the Mori patent in

rejecting claim 10. The Examiner stated, "Mori teaches the invention substantially as

claimed,...a unit...for capturing sequential of sets of system operation signals of said

integrated circuit [col. 2 lines 26-53];...a memory cache memory 1, Fig 3] coupled to said unit

and to said interface, said system operation signals stored in said memory at one or more clock

signal rates internal to said integrated circuit and retrieved from said memory through said

interface to said external process at one or more clock signal rates external to said integrated

circuit [col. 3 lines 10-28]; wherein said external diagnostics processor can process said

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captured system operation signals [external tester examines test results, see abstract]." With due respect to the Examiner, Mori is referring to <u>test</u> data (or more accurately, test results data), not system operation signals, as recited in the applicants' claims. The Mori patent teaches the use of the existing cache for test. See, for example, col. 5, lines 37-43; col. 7, lines 1-4. "After the completion of the test, the test results are transmitted from the data cache to the external tester under cache test mode." Col. 5, lines 7-10. This is not what claim 10 recites.

Hence claim 10 should be allowed. Likewise, claims 11-14 should be allowed for at least being dependent upon an allowable base claim. These claims are also allowable in their right. For example, dependent claim 11 recites, "...trigger logic responsive to said system operation signals for initiating storage of a set of said system operation signals in said memory." The Examiner cited the Gheewala patent as teaching "a trigger logic [see circuitry of Fig. 3 and the logic of TABLE A on col. 6 and TABLE B on col. 8] responsive to system operation signals for initiating/terminating storage of said system operation signals in said memory [when P1=0 and P2=0, S2 value is written into latch 68, when control signal C=1, the value then transmitted to driver 42, col. 7, lines 1-15]." Even assuming *arguendo* that the Gheewala interface circuit operates to store system operation signals, as called for by the applicants' claims, there is no teaching of any trigger logic, which is "responsive to said system operation signals for initiating storage...." The circuitry of Fig. 3 is the means by which storage is performed and the logic of TABLES A and B are the logic signals to manipulate the interface circuit of Fig. 3. There is no trigger logic circuitry described to initiate these logic signals, as called for in claim 11. Claim 11 should be allowed and, by the same reasoning, claim 12 should also be allowed. Claims 13 and 14 should be allowable by the same arguments made previously with respect to dependent claim 6.

Previously pending independent claim 15 was rejected for obviousness by the combination of the previously cited Rajki and Mori patents. The applicants have amended claim 15 to recite a method of operating an integrated circuit having logic blocks, comprising, "operating said logic blocks to perform system operations at one or more clock signal rates internal to said integrated circuit; enabling said probe lines responsive to said control unit to capture system operation signals of said logic blocks at one or more clock signal rates internal to said integrated circuit; retrieving said system operation signals from said logic blocks along

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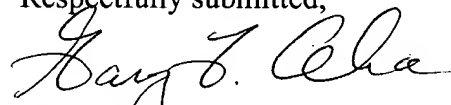Application No.: 09/275,726
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said probe lines at one or more clock signal rates internal to said integrated circuit, storing said system operation signals in said memory at one or more clock signal rates internal to said integrated circuit; and processing said stored system operation signals to perform test and debug operations of said logic blocks of said integrated circuit." Such steps are not found in the cited references as argued above. Note that what is being captured are system operation signals, not test signals.

Finally, the applicants have added new claims 16-22. Claims 16-18 are dependent upon independent claim 15; claim 19 is dependent upon independent claim 10; and claim 20 –22 are dependent upon independent claim 1. From the arguments above, it should be evident that these new claims are also allowable.

Therefore, in view of the amendments above and remarks thereto, the applicants respectfully request that the rejections be removed, that claims 1-22 be allowed and the case be passed to issue.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned attorney at 650-326-2400.

Respectfully submitted,

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